

Listing of Claims:

1. (Currently Amended) A synchroniser for use in a receiver which receives signals, said synchroniser comprising:

means for providing a digital control signal, said control signal defining a plurality of different levels;

means for controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values;

means for converting said digital control signal into an analog control signal for controlling a mixing frequency; and

means for estimating the difference between the levels of successive ones of said analog control signal signals.

2. (Canceled)

3. (Currently Amended) A The synchroniser as claimed in of claim 1, wherein said providing means, said controlling means and said estimating means are in the digital domain.

4. (Currently Amended) A The synchroniser as claimed in of claim 3, wherein said providing means, said controlling means and said estimating means are provided in a digital signal processor.

5. (Currently Amended) A The synchroniser as claimed in of claim 1, wherein said providing means comprises a digital corrector.

6. (Currently Amended) A The synchroniser as claimed in of claim 1, wherein a rough correction is provided by said control signal.

7. (Currently Amended) A The synchroniser as claimed in of claim 6, wherein a rough correction is provided in an ~~analogue~~ analog domain.

8. (Currently Amended) A The synchroniser ~~as claimed in~~ of claim 6, wherein a finer correction is provided.

9. (Currently Amended) A The synchroniser ~~as claimed in~~ of claim 8, wherein said finer correction is provided in a digital domain.

10. (Currently Amended) A The synchroniser ~~as claimed in~~ of claim 1, wherein said means for estimating comprises an estimator arranged to determine that the difference between two successive levels has increased if a difference between the upper of said levels and an estimated level for an actual signal provides a signal at a higher level than a signal provided by a difference between a lower of said levels and an estimated level for the actual signal.

11. (Currently Amended) A The synchroniser ~~as claimed in~~ of claim 2 1, wherein said means for estimating comprises an estimator arranged to determine that the difference between two successive levels has increased if a difference between the upper of said levels and an estimated level for an actual signal provides a signal at a higher level than a signal provided by a difference between a lower of said levels and an estimated level for the actual signal.

12. (Currently Amended) A The synchroniser ~~as claimed in~~ of claim 1, wherein said means for estimating comprises an estimator arranged to determine that an actual signal has changed if a difference between the upper of said levels and an actual signal provides a signal at substantially the same level as a signal provided by a difference between a lower of said levels and the actual signal, said same level being different to a previous level for said actual signal.

13. (Currently Amended) A The synchroniser ~~as claimed in~~ of claim 1, wherein said synchroniser is arranged to at least one of acquire and track frequency error.

14. (Currently Amended) A The synchroniser ~~as claimed in~~ of claim 1, wherein said synchroniser is arranged to at least one of acquire and track timing error.

15. (Currently Amended) A The receiver comprising a the synchroniser as claimed in claim 1.

16. (Canceled)

17. (Currently Amended) A The synchroniser ~~as claimed in~~ of claim 2 ~~1~~, wherein said providing means, said controlling means and said estimating means are in the digital domain.

18. (Currently Amended) A The synchroniser ~~as claimed in~~ of claim 7, wherein a finer correction is provided.

19. (Currently Amended) A The receiver ~~as claimed in~~ of claim 15, further comprising:

- an antenna for receiving signals;

- a first bandpass filter for filtering out unwanted signals;

- a mixer for downconverting received signals to a baseband frequency;

- a second bandpass filter for removing unwanted signals falling outside the bandwidth of said second bandpass filter;

- an ~~analogue~~ analog to digital converter for converting signals received from said second bandpass filter from ~~analogue~~ analog to digital form; and

- a digital to ~~analogue~~ analog converter for converting the signals received from said digital signal processor from digital to ~~analogue~~ analog form.

20. (Currently Amended) A The receiver ~~as claimed in~~ of claim 19, wherein said synchroniser includes a digital signal processor comprising:

- a detector for measuring frequency errors and sending a digital word;

- a filter for filtering said digital word output by said detector;

- a step size estimator for estimating an actual step size of a frequency change provided by said digital to ~~analogue~~ analog converter and providing said actual step size to ~~analogue~~ analog correction; and

- a digital automatic frequency control unit for controlling division of correction between ~~analogue~~ analog and digital parts, performing an accurate

correction so that a zero or close to zero error is achieved and compensating for the effect of an ~~analogue~~ analog control for which a step size is estimated while a control word is changed[[:]].

21. (Currently Amended) A method for providing synchronization in a receiver, comprising the steps of:

providing a digital control signal, said control signal defining a plurality of different levels;

controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values;

converting the digital control signal into an analog control signal for controlling a mixing frequency; and

estimating the difference between the levels of successive ones of said analog control signal signals.